

5 kV LED EMULATOR INPUT, OPEN COLLECTOR OUTPUT ISOLATORS

Features

- Pin-compatible, drop-in upgrades for popular high-speed digital optocouplers
- Performance and reliability advantages vs. optocouplers
 - Resistant to temperature, age and forward current effects
 - 10x lower FIT rate for longer service life
 - Higher common-mode transient immunity: >50 kV/μs typical
 - Lower power and forward input diode current
- PCB footprint compatible with optocoupler packaging
- Wide range of product options
 - 1 channel diode emulator input
 - 3 to 30 V open collector output
 - Propagation delay 30 ns
 - Data rates dc to 15 Mbps
 - Up to 5000 V_{RMS} isolation and 10 kV surge protection
 - AEC-Q100 qualified
 - Wide operating temperature range
 - -40 to +125 °C
 - RoHS-compliant packages
 - SOIC-8 (Narrow body)
 - DIP8 (Gull-wing)
 - SDIP6 (Stretched SO-6)
 - LGA8

Applications

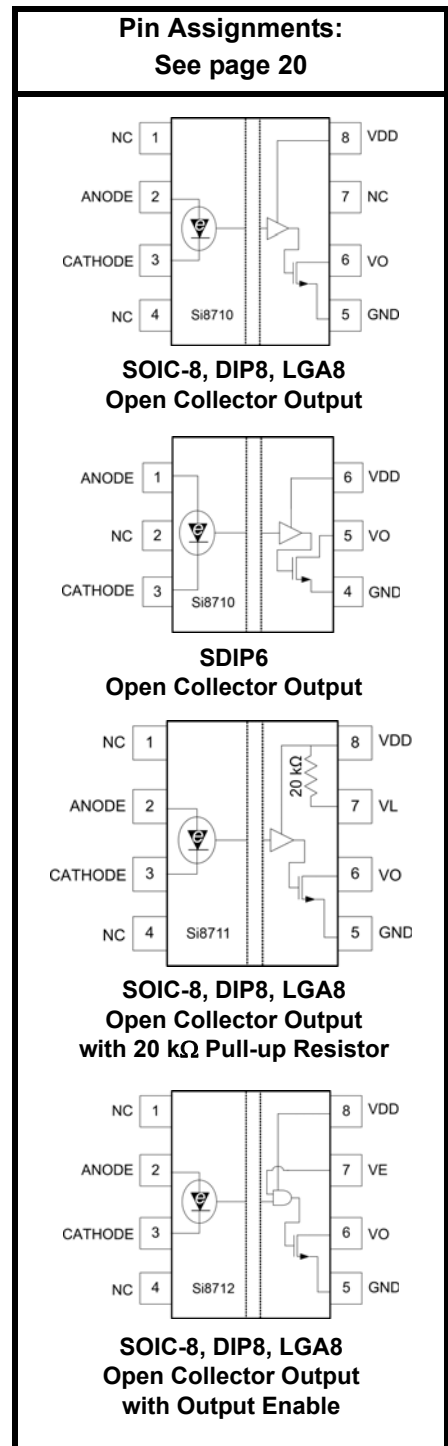
- Industrial automation
- Motor controls and drives
- Isolated switch mode power supplies
- Isolated data acquisition
- Test and measurement equipment

Safety Regulatory Approvals

- UL 1577 recognized
 - Up to 5000 Vrms for 1 minute
- CSA component notice 5A approval
 - IEC 60950-1, 61010-1, 60601-1 (reinforced insulation)
- VDE certification conformity
 - IEC60747-5-2/VDE0884 Part 10 (basic/reinforced insulation)
- CQC certification approval
 - GB4943.1

Description

The Si87xx isolators are pin-compatible, one-channel, drop-in replacements for popular optocouplers with data rates up to 15 Mbps. These devices isolate high-speed digital signals and offer performance, reliability, and flexibility advantages not available with optocoupler solutions. The Si87xx series is based on Silicon Labs' proprietary CMOS isolation technology for low-power and high-speed operation and are resistant to the wear-out effects found in optocouplers that degrade performance with increasing temperature, forward current, and device age. As a result, the Si87xx series offer longer service life and dramatically higher reliability compared to optocouplers. Ordering options include open collector output with and without integrated pull-up resistor and output enable options.



Patent pending

Si87xx

Functional Block Diagram

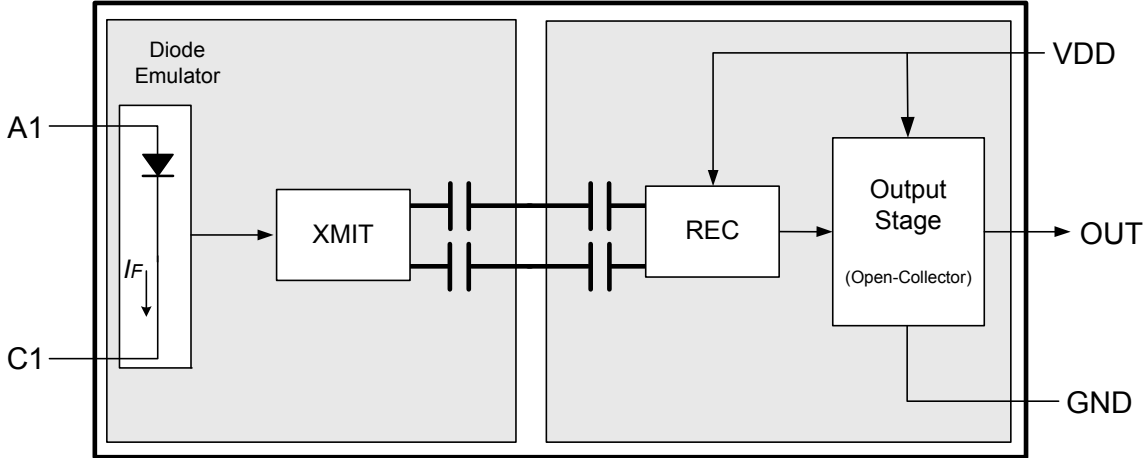


TABLE OF CONTENTS

| <u>Section</u> | <u>Page</u> |
|--|--------------------|
| 1. Electrical Specifications | 4 |
| 2. Functional Description | 14 |
| 2.1. Theory of Operation | 14 |
| 3. Technical Description | 15 |
| 3.1. Device Behavior | 15 |
| 3.2. Device Startup | 15 |
| 4. Applications | 16 |
| 4.1. Input Circuit Design | 16 |
| 4.2. Output Circuit Design and Power Supply Connections | 17 |
| 5. Pin Descriptions (SOIC-8, DIP8, LGA8) Open Collector | 18 |
| 6. Pin Descriptions (SOIC-8, DIP8, LGA8) Output Enable | 19 |
| 7. Pin Descriptions (SDIP6) Open Collector | 20 |
| 8. Pin Descriptions (SOIC-8, DIP8, LGA8) 20 kW Pull-Up Resistor | 21 |
| 9. Ordering Guide | 22 |
| 10. Package Outline: 8-Pin Narrow Body SOIC | 25 |
| 11. Land Pattern: 8-Pin Narrow Body SOIC | 26 |
| 12. Package Outline: DIP8 | 27 |
| 13. Land Pattern: DIP8 | 28 |
| 14. Package Outline: SDIP6 | 29 |
| 15. Land Pattern: SDIP6 | 31 |
| 16. Package Outline: LGA8 | 32 |
| 17. Land Pattern: LGA8 | 33 |
| 18. Top Markings | 34 |
| 18.1. Top Marking (8-Pin Narrow Body SOIC) | 34 |
| 18.2. Top Marking Explanation (8-Pin Narrow Body SOIC) | 34 |
| 18.3. Top Marking (DIP8) | 35 |
| 18.4. Top Marking Explanation (DIP8) | 35 |
| 18.5. Top Marking (SDIP6) | 36 |
| 18.6. Top Marking Explanation (SDIP6) | 36 |
| 18.7. Top Marking (LGA8) | 37 |
| 18.8. Top Marking Explanation (LGA8) | 37 |
| Document Change List | 38 |
| Contact Information | 39 |

Si87xx

1. Electrical Specifications

Table 1. Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---------------------------------|--------------------------------------|-----|-----|-----|------|
| V _{DD} Supply Voltage | V _{DD} | 3 | — | 30 | V |
| Input Current | I _{F(ON)} (see Figure 1) | 3 | — | 15 | mA |
| Si87xxA Devices | | 6 | — | 30 | mA |
| Si87xxB Devices | | 3 | — | 15 | mA |
| Si87xxC Devices | | | | | |
| Operating Temperature (Ambient) | T _A | -40 | — | 125 | °C |

Table 2. Electrical Characteristics

V_{DD} = 5 V; GND = 0 V; T_A = -40 to +125 °C; typical specs at 25 °C

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------------|---------------------|--|-------------|----------------------|-------------------|----------------|
| DC Parameters | | | | | | |
| Supply Voltage | V _{DD} | (V _{DD} -GND) | 3 | — | 30 | V |
| Supply Current | I _{DD} | Output high or low (V _{DD} = 5 to 30 V) | — | — | 1.7 | mA |
| Input Current Threshold | I _{F(TH)} | Si87xxA devices Si87xxB devices Si87xxC devices | — — — | — — — | 1.8 3.6 1.8 | mA mA mA |
| Input Current Hysteresis | I _{HYS} | Si87xxA devices Si87xxB devices Si87xxC devices | — — — | 0.17 0.34 0.17 | — — — | mA mA mA |
| Input Forward Voltage (OFF) | V _{F(OFF)} | Measured at ANODE with respect to CATHODE. | — | — | 1 | V |
| Input Forward Voltage (ON) | V _{F(ON)} | Measured at ANODE with respect to CATHODE. | 1.6 | — | 2.8 | V |
| Input Capacitance | C _I | f = 100 kHz V _F = 0 V, V _F = 2 V | — — | 15 15 | — — | pF pF |
| Logic Low Output Voltage | V _{OL} | I _{OL} = 3 mA, V _{DD} = 3.3 or 5 V I _{OL} = 13 mA, V _{DD} = 5.5 V | — — | — — | 0.4 0.7 | V V |
| Logic High Output Current | I _{OH} | V _{DD} = V _{OUT} = 5.5 V V _{DD} = V _{OUT} = 24 V | — — | — — | 0.5 1 | μA μA |
| Peak Output Current | I _{OPK} | Peak DC collector current drive (V _{DD} = 5 V) | — | 50 | — | mA |
| Output Low Impedance | R _{OL} | | — | — | 54 | Ω |
| Pull-up Resistor | R _{PU} | Using internal pull-up | — | 20 | — | kΩ |
| Enable High Min | V _{EH} | | 2 | — | 30 | V |
| Enable Low Max | V _{EL} | | — | — | 0.8 | V |
| Enable High Current Draw | I _{EH} | V _{DD} = V _{EH} = 5 V | — | 20 | — | μA |
| Enable Low Current Draw | I _{EL} | V _{DD} = 5 V, V _{EL} = 0 V | — | -10 | 0 | μA |

Table 2. Electrical Characteristics (Continued) $V_{DD} = 5\text{ V}$; $GND = 0\text{ V}$; $T_A = -40\text{ to }+125\text{ }^\circ\text{C}$; typical specs at $25\text{ }^\circ\text{C}$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|----------------|--|-----|-----|-----|-------------------|
| AC Switching Parameters ($V_{DD} = 5\text{ V}$, $R_L = 350\ \Omega$, $C_L = 15\text{ pF}$) | | | | | | |
| Maximum Data Rate | F_{DATA} | Si87xxA devices | DC | — | 15 | M _{BPS} |
| | | Si87xxB devices | DC | — | 15 | M _{BPS} |
| | | Si87xxC devices | DC | — | 1 | M _{BPS} |
| Minimum Pulse Width | MPW | Si87xxA devices | 66 | — | — | ns |
| | | Si87xxB devices | 66 | — | — | ns |
| | | Si87xxC devices | 1 | — | — | μs |
| Propagation Delay (Low-to-High) | t_{PLH} | $C_L = 15\text{ pF}$ using $350\ \Omega$ pull-up | — | — | 60 | ns |
| Propagation Delay (High-to-Low) | t_{PHL} | $C_L = 15\text{ pF}$ using $350\ \Omega$ pull-up | — | — | 60 | ns |
| Pulse Width Distortion | PWD | $ t_{PLH} - t_{PHL} $ | — | — | 20 | ns |
| Propagation Delay Skew | $t_{PSK(p-p)}$ | $t_{PSK(p-p)}$ is the magnitude of the difference in prop delays between different units operating at same supply voltage, load, and ambient temp. | — | — | 20 | ns |
| Rise Time | t_R | $C_L = 15\text{ pF}$ using $350\ \Omega$ pull-up | — | 15 | — | ns |
| Fall Time | t_F | $C_L = 15\text{ pF}$ using $350\ \Omega$ pull-up | — | 5 | — | ns |
| Device Startup Time | t_{START} | | — | — | 40 | μs |
| Common Mode Transient Immunity | CMTI | Output = low or high | | | | |
| | | $V_{CM} = 1500\text{ V}$ (See Figure 2) | | | | |
| | | $I_F = 3\text{ mA}$ for Si87xxA devices | 20 | 35 | — | kV/ μs |
| | | $I_F = 6\text{ mA}$ for Si87xxB devices | 35 | 50 | — | kV/ μs |
| | | $I_F = 3\text{ mA}$ for Si87xxC devices | 20 | 35 | — | kV/ μs |

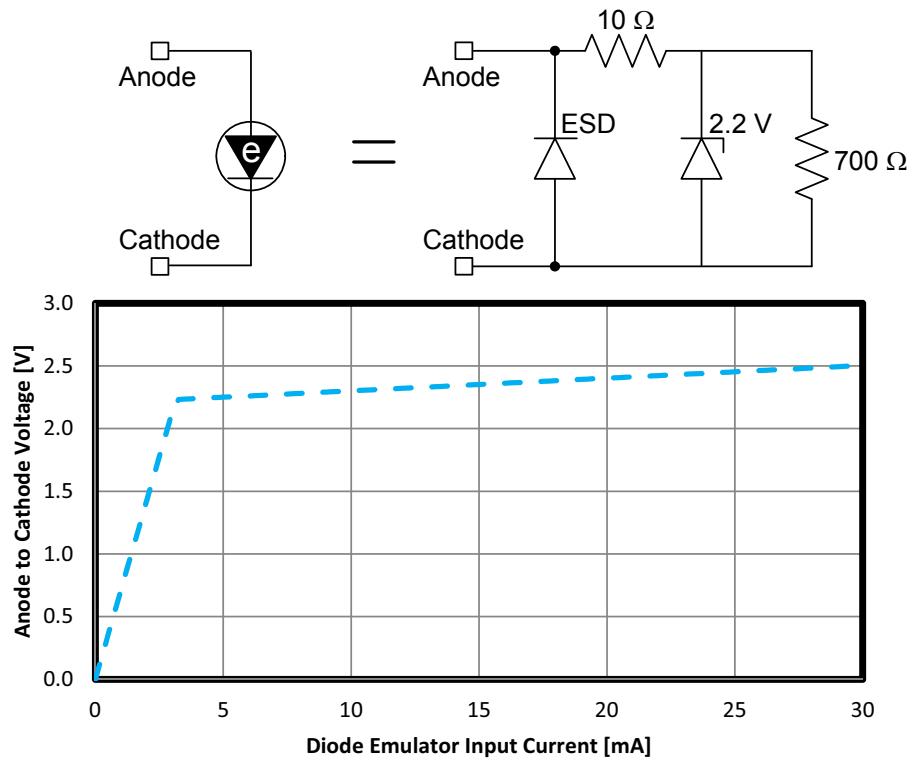


Figure 1. Diode Emulator Model and I-V Curve

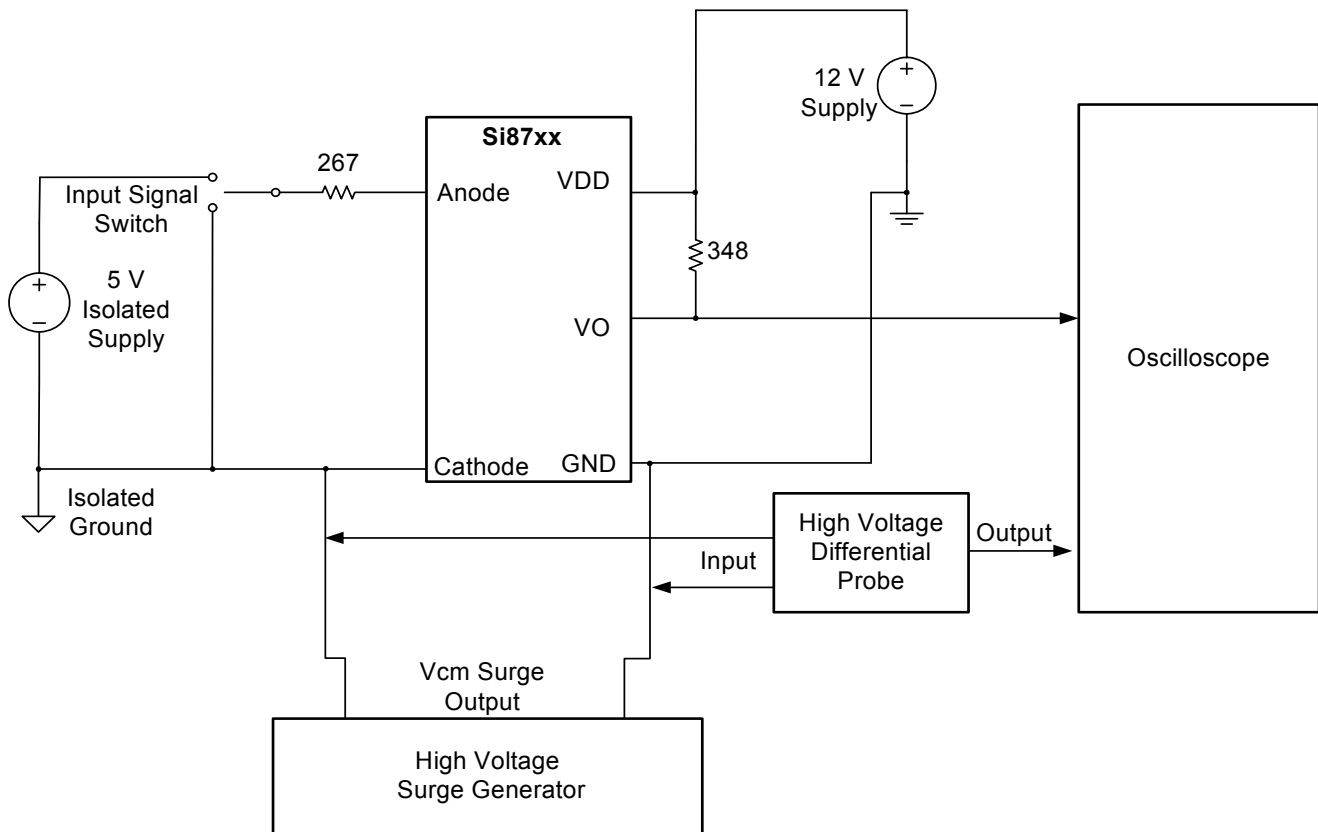


Figure 2. Common Mode Transient Immunity Characterization Circuit

Table 3. Regulatory Information*

| |
|---|
| CSA |
| The Si87xx is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873. |
| 61010-1: Up to 600 V _{RMS} reinforced insulation working voltage; up to 600 V _{RMS} basic insulation working voltage. |
| 60950-1: Up to 1000 V _{RMS} reinforced insulation working voltage; up to 1000 V _{RMS} basic insulation working voltage. |
| 60601-1: Up to 250 V _{RMS} reinforced insulation working voltage; up to 500 V _{RMS} basic insulation working voltage. |
| VDE |
| The Si87xx is certified according to IEC60747 and VDE0884. For more details, see File 5006301-4880-0001. |
| 60747-5-2: Up to 1414 V _{peak} for basic insulation working voltage. |
| VDE0884 Part 10: Up to 1414 V _{peak} for reinforced insulation working voltage. |
| UL |
| The Si87xx is certified under UL1577 component recognition program. For more details, see File E257455. |
| Rated up to 5000 V _{RMS} isolation voltage for basic protection. |
| CQC |
| The Si87xx is certified under GB4943.1-2011. For more details, see File V2012CQC001041. |
| Rated up to 1000 V _{RMS} reinforced insulation working voltage; up to 1000 V _{RMS} basic insulation working voltage. |
| *Note: Regulatory Certifications apply to 3.75 kV _{RMS} rated devices which are production tested to 4.5 kV _{RMS} for 1 sec. Regulatory Certifications apply to 5.0 kV _{RMS} rated devices which are production tested to 6.0 kV _{RMS} for 1 sec. For more information, see "9.Ordering Guide" on page 22. |

Table 4. Insulation and Safety-Related Specifications

| Parameter | Symbol | Test Condition | Value | | | | Unit |
|---|-----------------|----------------|------------------|------------------|------------------|------------------|------|
| | | | SOIC-8 | DIP8 | SDIP6 | LGA8 | |
| Nominal Air Gap (Clearance) | L(IO1) | | 4.7 min | 7.2 min | 9.6 min | 10.0 min | mm |
| Nominal External Tracking (Creepage) | L(IO2) | | 3.9 min | 7.0 min | 8.3 min | 10.0 min | mm |
| Minimum Internal Gap (Internal Clearance) | | | 0.016 | 0.016 | 0.016 | 0.016 | mm |
| Tracking Resistance (Proof Tracking Index) | PTI | IEC60112 | 600 | 600 | 600 | 600 | V |
| Erosion Depth | ED | | 0.031 | 0.031 | 0.057 | 0.021 | mm |
| Resistance (Input-Output)* | R _{IO} | | 10 ¹² | 10 ¹² | 10 ¹² | 10 ¹² | Ω |
| Capacitance (Input-Output)* | C _{IO} | f = 1 MHz | 1 | 1 | 1 | 1 | pF |
| *Note: To determine resistance and capacitance, the Si87xx is converted into a 2-terminal device. Pins 1–4 (1–3, SDIP6) are shorted together to form the first terminal, and pins 5–8 (4–6, SDIP6) are shorted together to form the second terminal. The parameters are then measured between these two terminals. | | | | | | | |

Table 5. IEC 60664-1 (VDE 0844 Part 2) Ratings

| Parameter | Test Condition | Specification | | | |
|-----------------------------|---|---------------|-------|-------|-------|
| | | SOIC-8 | DIP8 | SDIP6 | LGA8 |
| Basic Isolation Group | Material Group | I | I | I | I |
| Installation Classification | Rated Mains Voltages \leq 150 V _{RMS} | I-IV | I-IV | I-IV | I-IV |
| | Rated Mains Voltages \leq 300 V _{RMS} | I-IV | I-IV | I-IV | I-IV |
| | Rated Mains Voltages \leq 450 V _{RMS} | I-III | I-III | I-IV | I-IV |
| | Rated Mains Voltages \leq 600 V _{RMS} | I-III | I-III | I-IV | I-IV |
| | Rated Mains Voltages \leq 1000 V _{RMS} | — | — | — | I-III |

Table 6. IEC 60747-5-2 Insulation Characteristics*

| Parameter | Symbol | Test Condition | Characteristic | | | | Unit |
|--|-------------------|--|------------------|------------------|------------------|------------------|---------|
| | | | SOIC-8 | DIP8 | SDIP6 | LGA8 | |
| Maximum Working Insulation Voltage | V _{IORM} | | 630 | 891 | 1140 | 1414 | V peak |
| Input to Output Test Voltage | V _{PR} | Method b1 (V _{IORM} × 1.875 = V _{PR} , 100% Production Test, t _m = 1 sec, Partial Discharge < 5 pC) | 1181 | 1671 | 2138 | 2652 | V peak |
| Transient Overvoltage | V _{IOTM} | t = 60 sec | 6000 | 6000 | 8000 | 8000 | V peak |
| Surge Voltage | V _{IOSM} | 1.2 μs rise, 50 μs fall 50% | 10 | 10 | 10 | 10 | kV peak |
| Pollution Degree (DIN VDE 0110, Table 1) | | | 2 | 2 | 2 | 2 | |
| Insulation Resistance at T _S , V _{IO} = 500 V | R _S | | >10 ⁹ | >10 ⁹ | >10 ⁹ | >10 ⁹ | Ω |

***Note:** This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si87xx provides a climate classification of 40/125/21.

Table 7. IEC Safety Limiting Values

| Parameter | Symbol | Test Condition | Max | | | | Unit |
|------------------|--------|--|--------|------|-------|------|------|
| | | | SOIC-8 | DIP8 | SDIP6 | LGA8 | |
| Case Temperature | T_S | | 140 | 140 | 140 | 140 | °C |
| Input Current | I_S | $\theta_{JA} = 110\text{ °C/W (SOIC-8),}$ 110 °C/W (DIP8), 105 °C/W (SDIP6), 220 °C (LGA8), $V_F = 2.8\text{ V, } T_J = 140\text{ °C,}$ $T_A = 25\text{ °C}$ | 370 | 370 | 390 | 185 | mA |
| Output Power | P_S | | 1 | 1 | 1 | 0.5 | W |

Note: Maximum value allowed in the event of a failure; also see the thermal derating curve in Figures 3, 4, 5, and 6.

Table 8. Thermal Characteristics

| Parameter | Symbol | Typ | | | | Unit |
|---------------------------------------|---------------|--------|------|-------|------|-----------------------------|
| | | SOIC-8 | DIP8 | SDIP6 | LGA8 | |
| IC Junction-to-Air Thermal Resistance | θ_{JA} | 110 | 110 | 105 | 220 | $^{\circ}\text{C}/\text{W}$ |

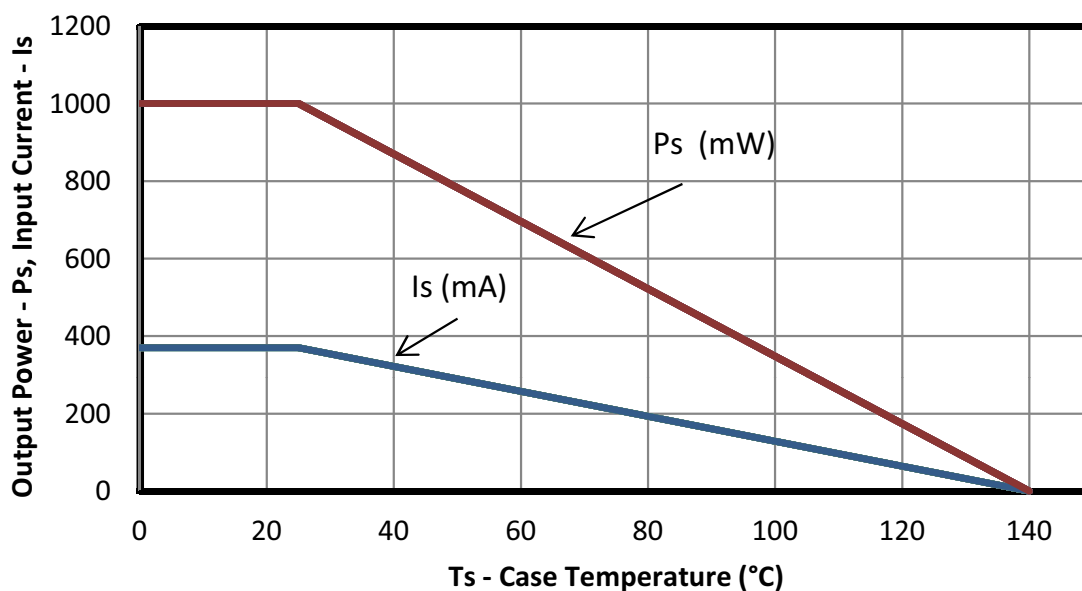


Figure 3. (SOIC-8) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2 and VDE0884 part 10

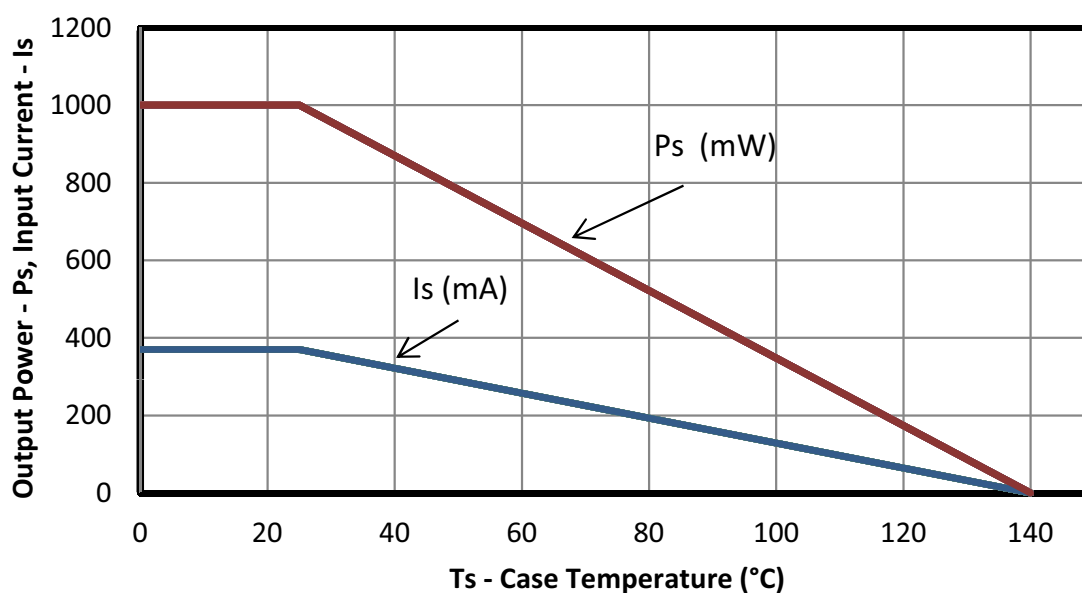


Figure 4. (DIP8) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2 and VDE0884 part 10

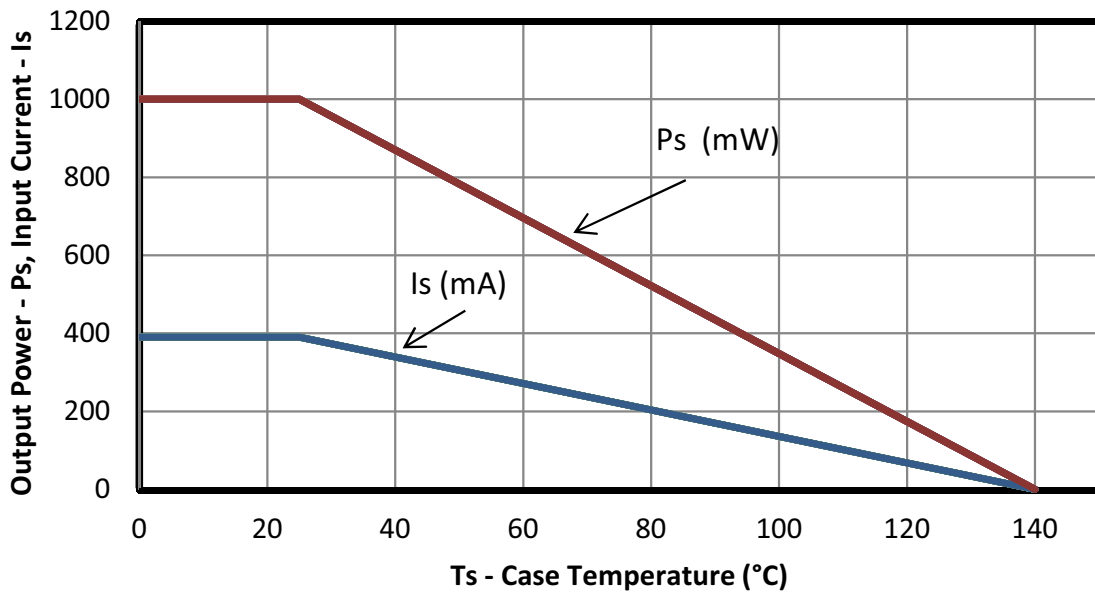


Figure 5. (SDIP6) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2 and VDE0884 part 10

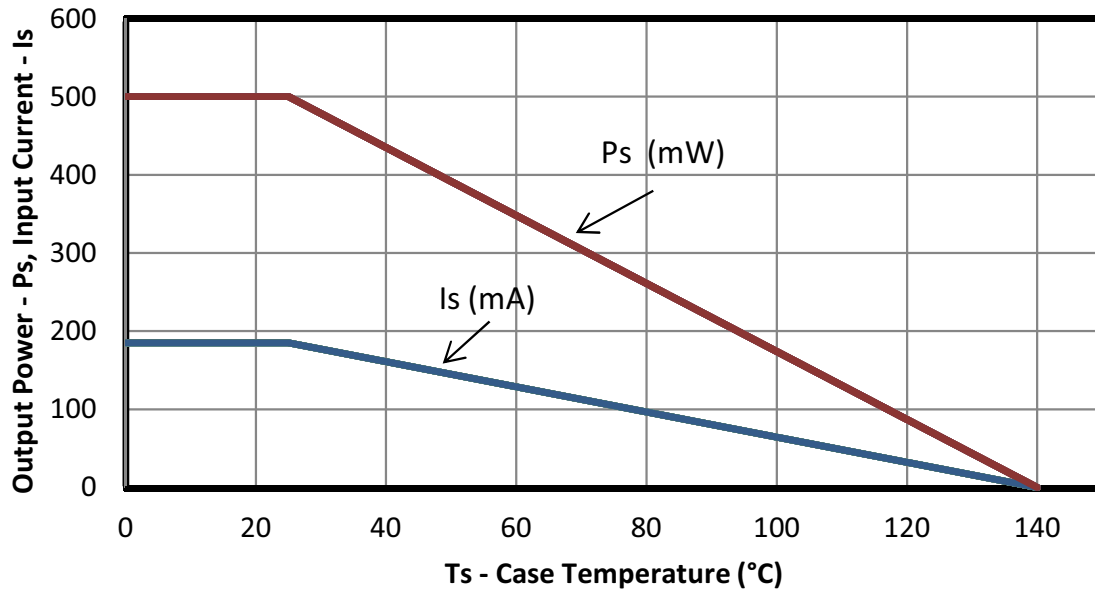


Figure 6. (LGA8) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2 and VDE0884 part 10

Table 9. Absolute Maximum Ratings*

| Parameter | Symbol | Min | Max | Unit |
|--|--------------|-------------|----------------|----------------|
| Storage Temperature | T_{STG} | -65 | +150 | °C |
| Operating Temperature | T_A | -40 | +125 | °C |
| Junction Temperature | T_J | — | +140 | °C |
| Average Forward Input Current Si87xxA Devices Si87xxB Devices Si87xxC Devices | $I_{F(AVG)}$ | — — — | 15 30 15 | mA mA mA |
| Peak Transient Input Current ($< 1 \mu s$ pulse width, 300 ps) | I_{FTR} | — | 1 | A |
| Reverse Input Voltage | V_R | — | 0.3 | V |
| Supply Voltage | V_{DD} | -0.5 | 36 | V |
| Output Voltage | V_{OUT} | -0.5 | 36 | V |
| Enable Voltage | V_{OUT} | -0.5 | $V_{DD}+0.5$ | V |
| Output Sink Current | I_{SINK} | — | 15 | mA |
| Average Output Current | $I_{O(AVG)}$ | — | 8 | mA |
| Peak Output Current ($V_{DD} = 5 V$) | I_{OPK} | — | 75 | mA |
| Input Power Dissipation | P_I | — | 90 | mW |
| Output Power Dissipation | P_O | — | 50 | mW |
| Total Power Dissipation | P_T | — | 140 | mW |
| Lead Solder Temperature (10 s) | | — | 260 | °C |
| HBM Rating ESD | | 3 | — | kV |
| Machine Model ESD | | 200 | — | V |
| CDM | | 500 | — | V |
| Maximum Isolation Voltage (1 s) SOIC-8 | | — | 4500 | V_{RMS} |
| Maximum Isolation Voltage (1 s) DIP8 | | — | 4500 | V_{RMS} |
| Maximum Isolation Voltage (1 s) SDIP6 | | — | 6500 | V_{RMS} |
| Maximum Isolation Voltage (1 s) LGA8 | | — | 6500 | V_{RMS} |

***Note:** Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions specified in the operational sections of this data sheet.

2. Functional Description

2.1. Theory of Operation

The Si87xx are pin-compatible, one-channel, drop-in replacements for popular optocouplers with data rates up to 15 Mbps. The operation of an Si87xx channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for the Si87xx is shown in Figure 7.

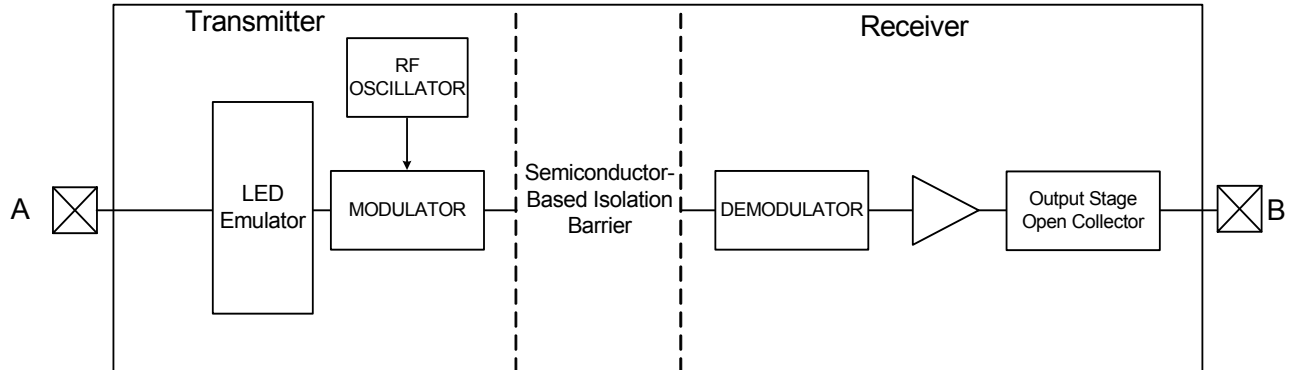


Figure 7. Simplified Channel Diagram

3. Technical Description

3.1. Device Behavior

Truth tables for the Si87xx are summarized in Table 10.

Table 10. Si87xx Truth Table Summary¹

| Input | V _{DD} | EN ² | V _O ³ |
|-------|-----------------|-----------------|-----------------------------|
| OFF | > UVLO | H | HIGH |
| OFF | > UVLO | L | HIGH |
| OFF | < UVLO | H | HIGH |
| OFF | < UVLO | L | HIGH |
| ON | > UVLO | H | LOW |
| ON | > UVLO | L | HIGH |
| ON | < UVLO | H | HIGH |
| ON | < UVLO | L | HIGH |

Notes:

1. This truth table assumes V_{DD} is powered. UVLO is typically 2.8 V.
2. Si8712 only.
3. The output voltage level is determined by the external pull-up supply.

3.2. Device Startup

During start-up, Output V_O floats and its voltage level is determined by the external pull-up until V_{DD} rises above the UVLO+ threshold for a minimum time period of t_{START}. Following this, the output is low when the current flowing from anode to cathode is > I_{F(ON)}. Device startup, normal operation, and shutdown behavior is shown in Figure 8.

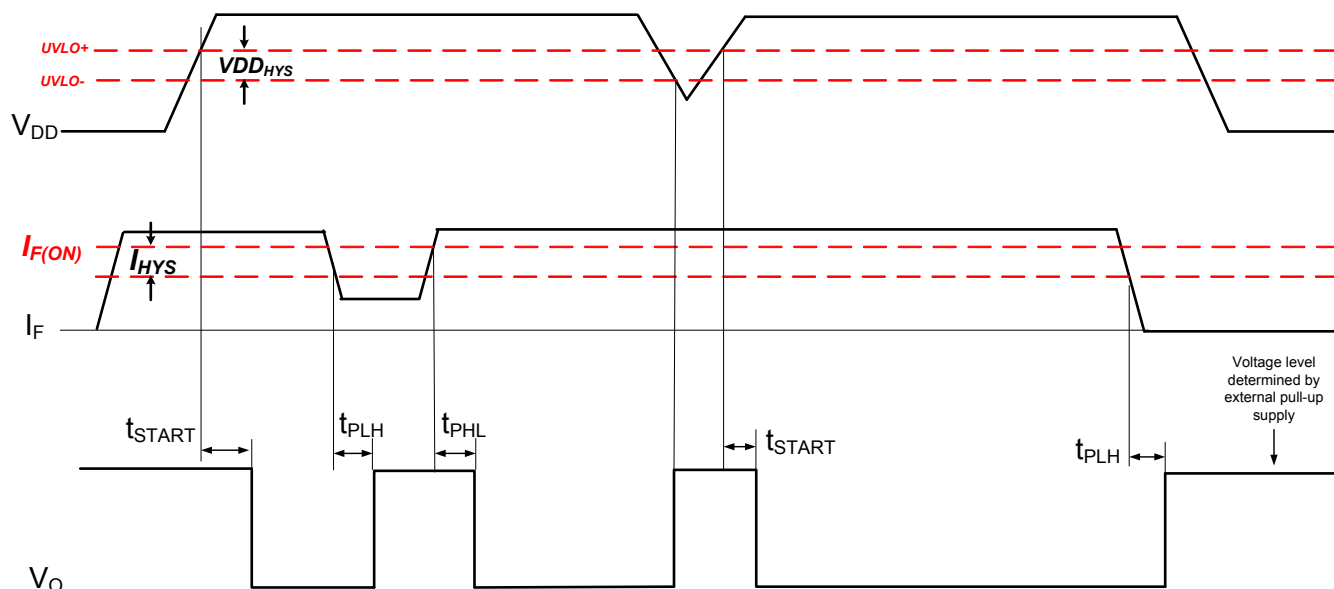


Figure 8. Si87xx Operating Behavior ($I_F \geq I_{F(MIN)}$ when $V_F \geq V_{F(MIN)}$)

4. Applications

The following sections detail the input and output circuits necessary for proper operation of the Si87xx family.

4.1. Input Circuit Design

Opto coupler manufacturers typically recommend the circuits shown in Figures 9 and 10. These circuits are specifically designed to improve opto-coupler input common-mode rejection and increase noise immunity.

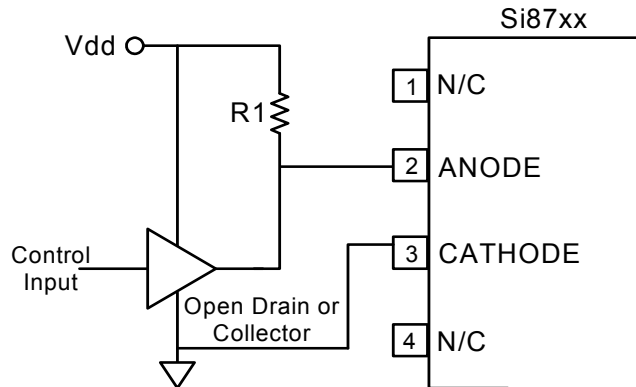


Figure 9. Si87xx Input Circuit

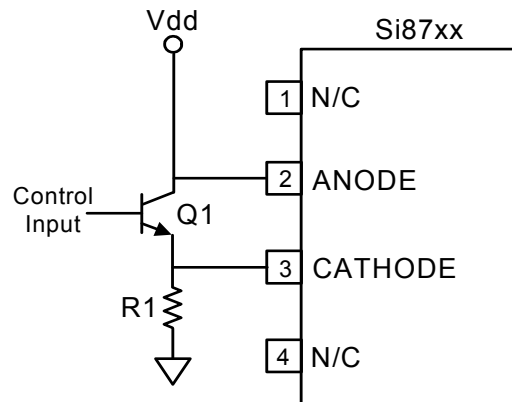


Figure 10. High CMR Si87xx Input Circuit

The optically-coupled circuit of Figure 9 turns the LED on when the control input is high. However, internal capacitive coupling from the LED to the power and ground conductors can momentarily force the LED into its off state when the anode and cathode inputs are subjected to a high common-mode transient. The circuit shown in Figure 10 addresses this issue by using a value of R1 sufficiently low to overdrive the LED, ensuring it remains on during an input common-mode transient. Q1 shorts the LED off in the low output state, again increasing common-mode transient immunity.

Some opto coupler applications recommend reverse-biasing the LED when the control input is off to prevent coupled noise from energizing the LED. The Si87xx input circuit requires less current and has twice the off-state noise margin compared to opto couplers. However, high CMR opto coupler designs that overdrive the LED (see Figure 10) may require increasing the value of R1 to limit input current I_F to its maximum rating when using the Si87xx. In addition, there is no benefit in driving the Si87xx input diode into reverse bias when in the off state. Consequently, opto coupler circuits using this technique should either leave the negative bias circuitry unpopulated or modify the circuitry (e.g., add a clamp diode or current limiting resistor) to ensure that the anode pin of the Si87xx is no more than -0.3 V with respect to the cathode when reverse-biased.

New designs should consider the input circuit configurations of Figure 11, which are more efficient than those of Figures 9 and 10. As shown, S1 and S2 represent any suitable switch, such as a BJT or MOSFET, analog transmission gate, processor I/O, etc. Also, note that the Si87xx input can be driven from the I/O port of any MCU or FPGA capable of sourcing a minimum of 6 mA (see Figure 11B). Additionally, note that the Si87xx propagation delay and output drive do not significantly change for values of I_F between $I_{F(MIN)}$ and $I_{F(MAX)}$.

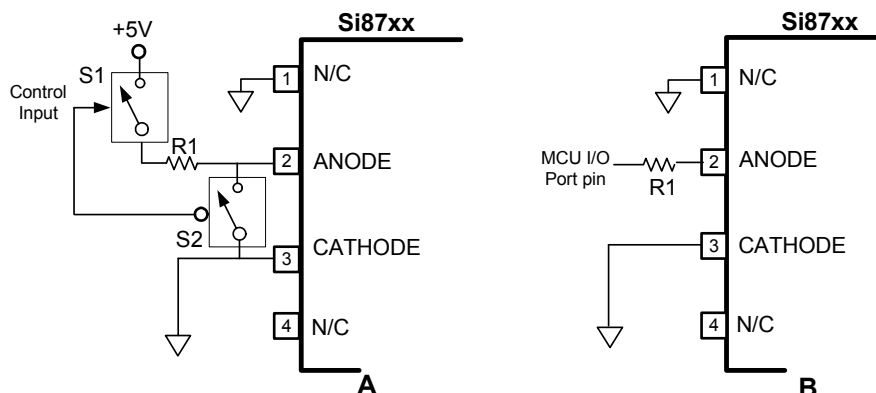


Figure 11. Si87xx Other Input Circuit Configurations

4.2. Output Circuit Design and Power Supply Connections

The speed of the open collector circuit is dependent upon the supply, V_{CC} , the pullup resistor, R_L , and the load modeled by C_L . Figure 12 illustrates three common circuit output configurations. For $V_{DD} = 5\text{ V}$ operation, $R_L > 350\ \Omega$ is recommended to ensure proper V_{OL} levels. For $V_{DD} = 30\text{ V}$ operation, $R_L > 2.1\text{ k}\Omega$ is recommended to ensure proper V_{OL} levels. If the enable pin is used (see Figure 12B) and two separate supplies power V_{DD} and the V_O pullup resistor, the enable pin should be referenced to the V_{DD} pin because V_O cannot exceed V_{DD} by more than 0.5 V. Figure 12C illustrates a circuit using the internal 20 k Ω resistor.

Note that GND can be biased at, above, or below ground as long as the voltage on V_{DD} with respect to GND is a maximum of 30 V. V_{DD} decoupling capacitors should be placed as close to the package pins as possible. The optimum values for these capacitors depend on load current and the distance between the chip and its power source. It is recommended that 0.1 and 1 μF bypass capacitors be used to reduce high-frequency noise and maximize performance. Opto replacement applications should limit their supply voltages to 30 V or less.

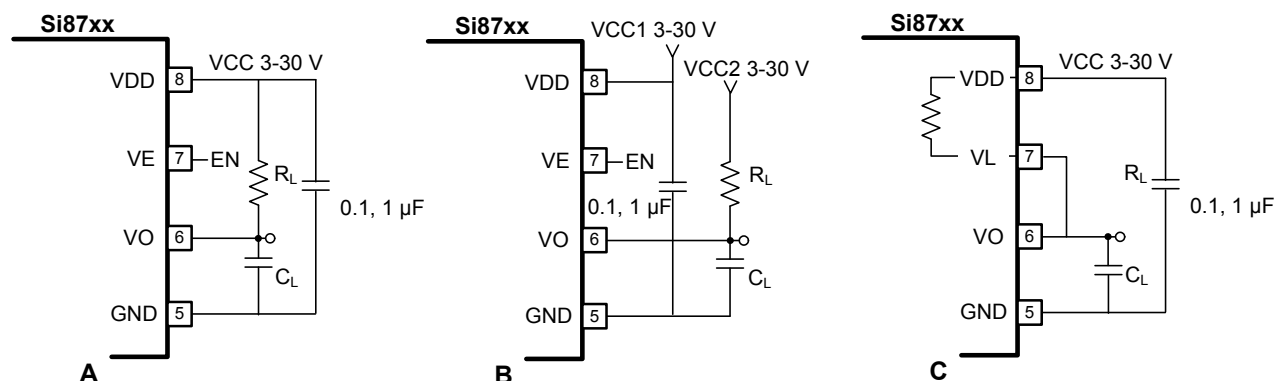


Figure 12. Si87xx Output Circuit Configurations

5. Pin Descriptions (SOIC-8, DIP8, LGA8) Open Collector

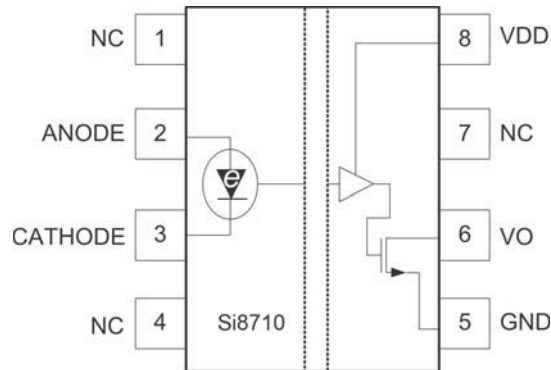


Figure 13. Pin Configuration

Table 11. Pin Descriptions (SOIC-8, DIP8, LGA8) Open Collector

| Pin | Name | Description |
|-----|----------|---|
| 1 | NC* | No connect. |
| 2 | ANODE | Anode of LED emulator. V_O follows the signal applied to this input with respect to the CATHODE input. |
| 3 | CATHODE | Cathode of LED emulator. V_O follows the signal applied to ANODE with respect to this input. |
| 4 | NC* | No connect. |
| 5 | GND | External MOSFET source connection and ground reference for V_{DD} . This terminal is typically connected to ground but may be tied to a negative or positive voltage. |
| 6 | V_O | Output signal. |
| 7 | NC* | No connect. |
| 8 | V_{DD} | Output-side power supply input referenced to GND (30 V max). |

***Note:** No Connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane.

6. Pin Descriptions (SOIC-8, DIP8, LGA8) Output Enable

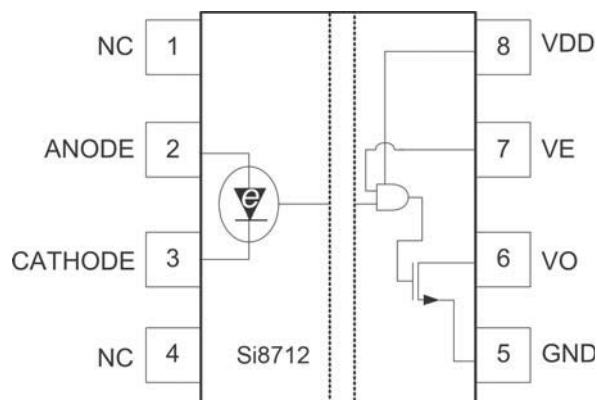


Figure 14. Pin Configuration

Table 12. Pin Descriptions (SOIC-8, DIP8, LGA8) Output Enable

| Pin | Name | Description |
|-----|----------|---|
| 1 | NC* | No connect. |
| 2 | ANODE | Anode of LED emulator. V_O follows the signal applied to this input with respect to the CATHODE input. |
| 3 | CATHODE | Cathode of LED emulator. V_O follows the signal applied to ANODE with respect to this input. |
| 4 | NC* | No connect. |
| 5 | GND | External MOSFET source connection and ground reference for V_{DD} . This terminal is typically connected to ground but may be tied to a negative or positive voltage. |
| 6 | V_O | Output signal. |
| 7 | V_E | Output enable. Tied to V_{DD} to enable output. |
| 8 | V_{DD} | Output-side power supply input referenced to GND (30 V max). |

***Note:** No Connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane.

7. Pin Descriptions (SDIP6) Open Collector

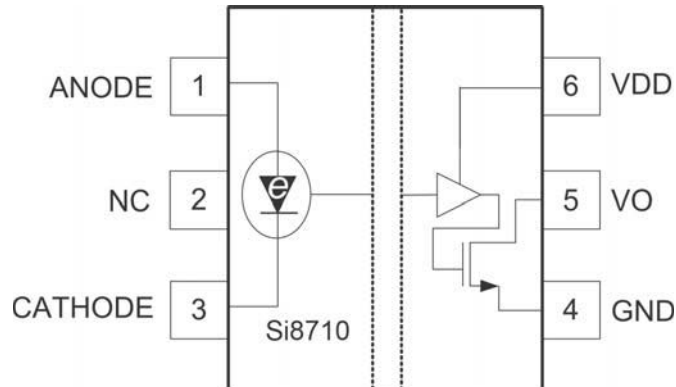


Figure 15. Pin Configuration

Table 13. Pin Descriptions (SDIP6) Open Collector

| Pin | Name | Description |
|-----|----------|---|
| 1 | ANODE | Anode of LED emulator. V_O follows the signal applied to this input with respect to the CATHODE input. |
| 2 | NC* | No connect. |
| 3 | CATHODE | Cathode of LED emulator. V_O follows the signal applied to ANODE with respect to this input. |
| 4 | GND | External MOSFET source connection and ground reference for V_{DD} . This terminal is typically connected to ground but may be tied to a negative or positive voltage. |
| 5 | V_O | Output signal. |
| 6 | V_{DD} | Output-side power supply input referenced to GND (30 V max). |

***Note:** No Connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane.

8. Pin Descriptions (SOIC-8, DIP8, LGA8) 20 k Ω Pull-Up Resistor

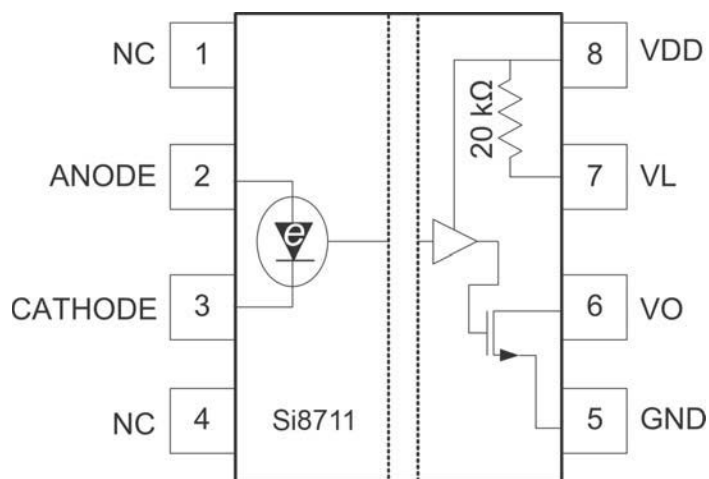


Figure 16. Pin Configuration

Table 14. Pin Descriptions (SOIC-8, DIP8, LGA8) 20 k Ω Pull-Up Resistor

| Pin | Name | Description |
|-----|----------|---|
| 1 | NC* | No connect. |
| 2 | ANODE | Anode of LED emulator. V_O follows the signal applied to this input with respect to the CATHODE input. |
| 3 | CATHODE | Cathode of LED emulator. V_O follows the signal applied to ANODE with respect to this input. |
| 4 | NC* | No connect. |
| 5 | GND | External MOSFET source connection and ground reference for V_{DD} . This terminal is typically connected to ground but may be tied to a negative or positive voltage. |
| 6 | V_O | Output signal. |
| 7 | V_L | Output Pull-Up Load. Tie to V_O to enable load. |
| 8 | V_{DD} | Output-side power supply input referenced to GND (30 V max). |

***Note:** No Connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane.

9. Ordering Guide

Table 15. Si87xx Ordering Guide^{1,2,3}

| New Ordering Part Number (OPN) | Ordering Options | | | | |
|---|--|---|-------------------|----------------|----------|
| | Input/Output Configuration | Data Rate (Cross Reference) | Insulation Rating | Temp Range | Pkg Type |
| Open Collector Output (Available in SOIC-8, DIP8, and SDIP6) | | | | | |
| Si8710AC-B-IS | LED input Open collector output | 15 Mbps ACPL-W611, PS9303L2 (Functional Match) | 3.75 kVrms | -40 to +125 °C | SOIC-8 |
| Si8710BC-B-IS | High CMTI LED input Open collector output | 15 Mbps ACPL-W611, PS9303L2 (Functional Match) | 3.75 kVrms | -40 to +125 °C | SOIC-8 |
| Si8710CC-B-IS | LED input Open collector output | 1 Mbps ACPL-W611, PS9303L2 (Functional Match) | 3.75 kVrms | -40 to +125 °C | SOIC-8 |
| Si8710AC-B-IP | LED input Open collector output | 15 Mbps HCPL-4502 | 3.75 kVrms | -40 to +125 °C | DIP8/GW |
| Si8710BC-B-IP | High CMTI LED input Open collector output | 15 Mbps HCPL-4502 | 3.75 kVrms | -40 to +125 °C | DIP8/GW |
| Si8710CC-B-IP | LED input Open collector output | 1 Mbps HCPL-4502 | 3.75 kVrms | -40 to +125 °C | DIP8/GW |
| Si8710AD-B-IS | LED input Open collector output | 15 Mbps ACPL-W611, PS9303L2 | 5.0 kVrms | -40 to +125 °C | SDIP6 |
| Si8710BD-B-IS | High CMTI LED input Open collector output | 15 Mbps ACPL-W611, PS9303L2 | 5.0 kVrms | -40 to +125 °C | SDIP6 |
| Si8710CD-B-IS | LED input Open collector output | 1 Mbps ACPL-W611, PS9303L2 | 5.0 kVrms | -40 to +125 °C | SDIP6 |
| Notes: | | | | | |
| <ol style="list-style-type: none"> 1. All packages are RoHS-compliant with peak solder reflow temperatures of 260 °C according to the JEDEC industry standard classifications. 2. "Si" and "SI" are used interchangeably. 3. AEC-Q100 qualified. | | | | | |

Table 15. Si87xx Ordering Guide^{1,2,3} (Continued)

| New Ordering Part Number (OPN) | Ordering Options | | | | |
|---|---|--|-------------------|----------------|----------|
| | Input/Output Configuration | Data Rate (Cross Reference) | Insulation Rating | Temp Range | Pkg Type |
| Open Collector Output with 20 kΩ Pullup Resistor (Available in SOIC-8, DIP8, and LGA8) | | | | | |
| Si8711AC-B-IS | LED input Open collector output with integrated pullup | 15 Mbps HCPL-4506 (Functional Match) | 3.75 kVrms | -40 to +125 °C | SOIC-8 |
| Si8711BC-B-IS | High CMTI LED input Open collector output with integrated pullup | 15 Mbps HCPL-4506 (Functional Match) | 3.75 kVrms | -40 to +125 °C | SOIC-8 |
| Si8711CC-B-IS | LED input Open collector output with integrated pullup | 1 Mbps HCPL-4506 (Functional Match) | 3.75 kVrms | -40 to +125 °C | SOIC-8 |
| Si8711AC-B-IP | LED input Open collector output with integrated pullup | 15 Mbps HCPL-4506 | 3.75 kVrms | -40 to +125 °C | DIP8/GW |
| Si8711BC-B-IP | High CMTI LED input Open collector output with integrated pullup | 15 Mbps HCPL-4506 | 3.75 kVrms | -40 to +125 °C | DIP8/GW |
| Si8711CC-B-IP | LED input Open collector output with integrated pullup | 1 Mbps HCPL-4506 | 3.75 kVrms | -40 to +125 °C | DIP8/GW |
| Si8711AD-B-IM | LED input Open collector output with integrated pullup | 15 Mbps HCNW-4506 | 5.0 kVrms | -40 to +125 °C | LGA8 |
| Si8711BD-B-IM | High CMTI LED input Open collector output with integrated pullup | 15 Mbps HCNW-4506 | 5.0 kVrms | -40 to +125 °C | LGA8 |
| Si8711CD-B-IM | LED input Open collector output with integrated pullup | 1 Mbps HCNW-4506 | 5.0 kVrms | -40 to +125 °C | LGA8 |
| Notes: | | | | | |
| 1. All packages are RoHS-compliant with peak solder reflow temperatures of 260 °C according to the JEDEC industry standard classifications. | | | | | |
| 2. "Si" and "SI" are used interchangeably. | | | | | |
| 3. AEC-Q100 qualified. | | | | | |

Table 15. Si87xx Ordering Guide^{1,2,3} (Continued)

| New Ordering Part Number (OPN) | Ordering Options | | | | |
|---|--|---|-------------------|----------------|----------|
| | Input/Output Configuration | Data Rate (Cross Reference) | Insulation Rating | Temp Range | Pkg Type |
| Open Collector Output with Output Enable (Available in SOIC-8, DIP8, and LGA8) | | | | | |
| Si8712AC-B-IS | LED input Open collector output with enable | 15 Mbps HCPL-261x/260x (Functional Match) | 3.75 kVrms | -40 to +125 °C | SOIC-8 |
| Si8712BC-B-IS | High CMTI LED input Open collector output with enable | 15 Mbps HCPL-261x/260x (Functional Match) | 3.75 kVrms | -40 to +125 °C | SOIC-8 |
| Si8712CC-B-IS | LED input Open collector output with enable | 1 Mbps HCPL-261x/260x (Functional Match) | 3.75 kVrms | -40 to +125 °C | SOIC-8 |
| Si8712AC-B-IP | LED input Open collector output with enable | 15 Mbps HCPL-261x/260x | 3.75 kVrms | -40 to +125 °C | DIP8/GW |
| Si8712BC-B-IP | High CMTI LED input Open collector output with enable | 15 Mbps HCPL-261x/260x | 3.75 kVrms | -40 to +125 °C | DIP8/GW |
| Si8712CC-B-IP | LED input Open collector output with enable | 1 Mbps HCPL-261x/260x | 3.75 kVrms | -40 to +125 °C | DIP8/GW |
| Si8712AD-B-IM | LED input Open collector output with enable | 15 Mbps HCNW-2611 | 5.0 kVrms | -40 to +125 °C | LGA8 |
| Si8712BD-B-IM | High CMTI LED input Open collector output with enable | 15 Mbps HCNW-2611 | 5.0 kVrms | -40 to +125 °C | LGA8 |
| Si8712CD-B-IM | LED input Open collector output with enable | 1 Mbps HCNW-2611 | 5.0 kVrms | -40 to +125 °C | LGA8 |
| Notes: | | | | | |
| <ol style="list-style-type: none"> 1. All packages are RoHS-compliant with peak solder reflow temperatures of 260 °C according to the JEDEC industry standard classifications. 2. "Si" and "SI" are used interchangeably. 3. AEC-Q100 qualified. | | | | | |

10. Package Outline: 8-Pin Narrow Body SOIC

Figure 17 illustrates the package details for the Si87xx in an 8-pin narrow-body SOIC package. Table 16 lists the values for the dimensions shown in the illustration.

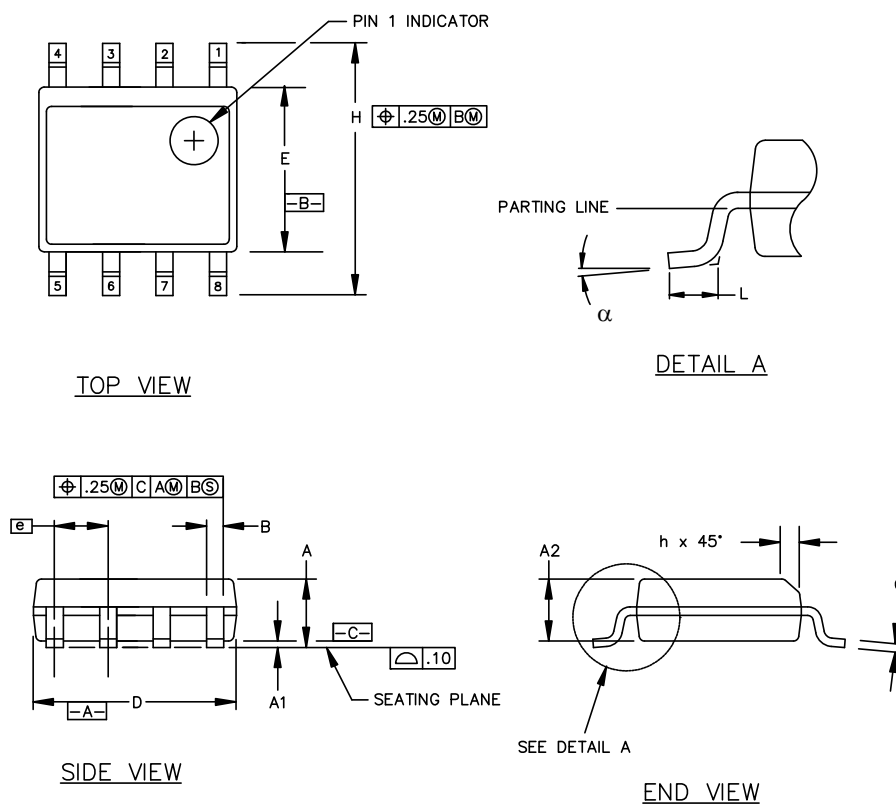


Figure 17. 8-Pin Narrow Body SOIC Package

Table 16. 8-Pin Narrow Body SOIC Package Diagram Dimensions

| Symbol | Millimeters | |
|----------|-------------|----------|
| | Min | Max |
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| A2 | 1.40 REF | 1.55 REF |
| B | 0.33 | 0.51 |
| C | 0.19 | 0.25 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.27 BSC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.27 |
| α | 0° | 8° |

11. Land Pattern: 8-Pin Narrow Body SOIC

Figure 18 illustrates the recommended land pattern details for the Si87xx in an 8-pin narrow-body SOIC. Table 17 lists the values for the dimensions shown in the illustration.

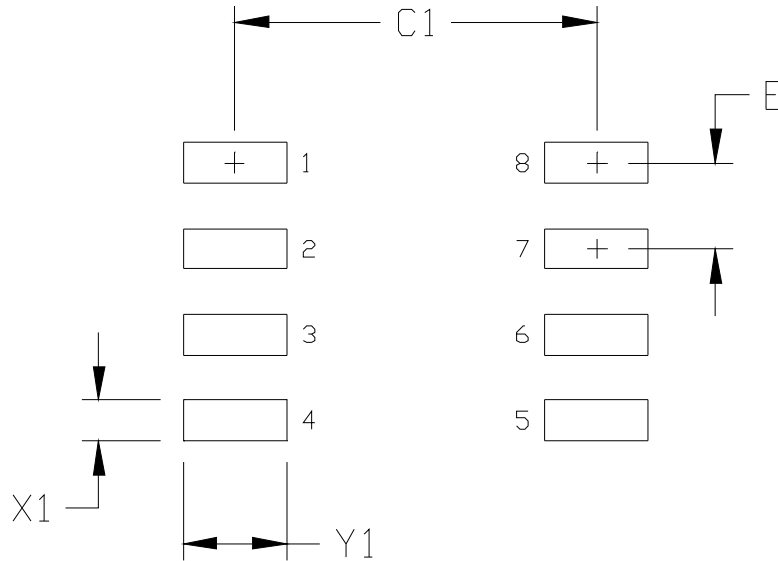


Figure 18. 8-Pin Narrow Body SOIC Land Pattern

Table 17. 8-Pin Narrow Body SOIC Land Pattern Dimensions

| Dimension | Feature | (mm) |
|---|--------------------|------|
| C1 | Pad Column Spacing | 5.40 |
| E | Pad Row Pitch | 1.27 |
| X1 | Pad Width | 0.60 |
| Y1 | Pad Length | 1.55 |
| Notes: | | |
| <ol style="list-style-type: none"> 1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion). 2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed. | | |

12. Package Outline: DIP8

Figure 19 illustrates the package details for the Si87xx in a DIP8 package. Table 18 lists the values for the dimensions shown in the illustration.

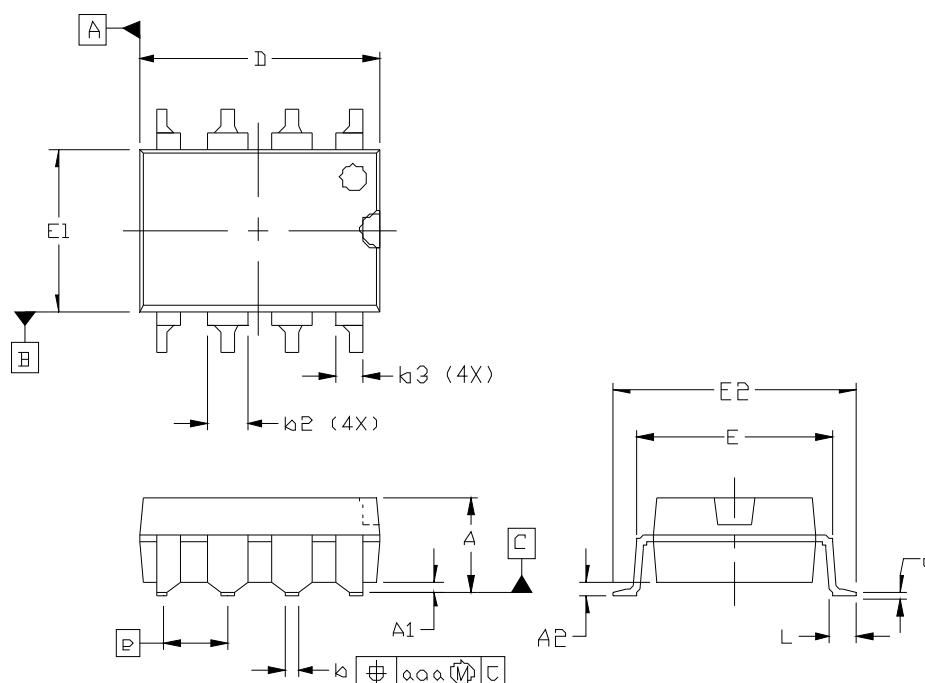


Figure 19. DIP8 Package

Table 18. DIP8 Package Diagram Dimensions

| Dimension | Min | Max |
|-----------|-----------|------|
| A | — | 4.19 |
| A1 | 0.55 | 0.75 |
| A2 | 3.17 | 3.43 |
| b | 0.35 | 0.55 |
| b2 | 1.14 | 1.78 |
| b3 | 0.76 | 1.14 |
| c | 0.20 | 0.33 |
| D | 9.40 | 9.90 |
| E | 7.37 | 7.87 |
| E1 | 6.10 | 6.60 |
| E2 | 9.40 | 9.90 |
| e | 2.54 BSC. | |
| L | 0.38 | 0.89 |
| aaa | — | 0.25 |

Notes:

- All dimensions shown are in millimeters (mm) unless otherwise noted.
- Dimensioning and Tolerancing per ANSI Y14.5M-1994.

13. Land Pattern: DIP8

Figure 20 illustrates the recommended land pattern details for the Si87xx in a DIP8 package. Table 19 lists the values for the dimensions shown in the illustration.

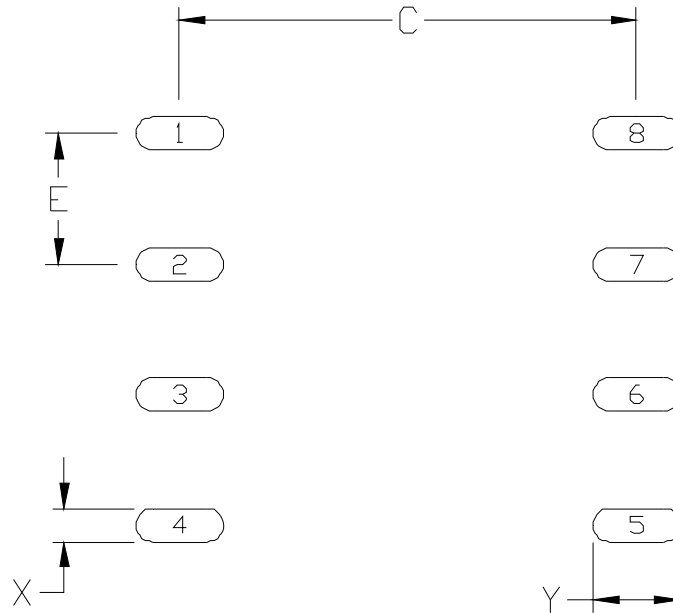


Figure 20. DIP8 Land Pattern

Table 19. DIP8 Land Pattern Dimensions*

| Dimension | Min | Max |
|--|----------|------|
| C | 8.85 | 8.90 |
| E | 2.54 BSC | |
| X | 0.60 | 0.65 |
| Y | 1.65 | 1.70 |
| *Note: This Land Pattern Design is based on the IPC-7351 specification. | | |

14. Package Outline: SDIP6

Figure 21 illustrates the package details for the Si87xx in an SDIP6 package. Table 20 lists the values for the dimensions shown in the illustration.

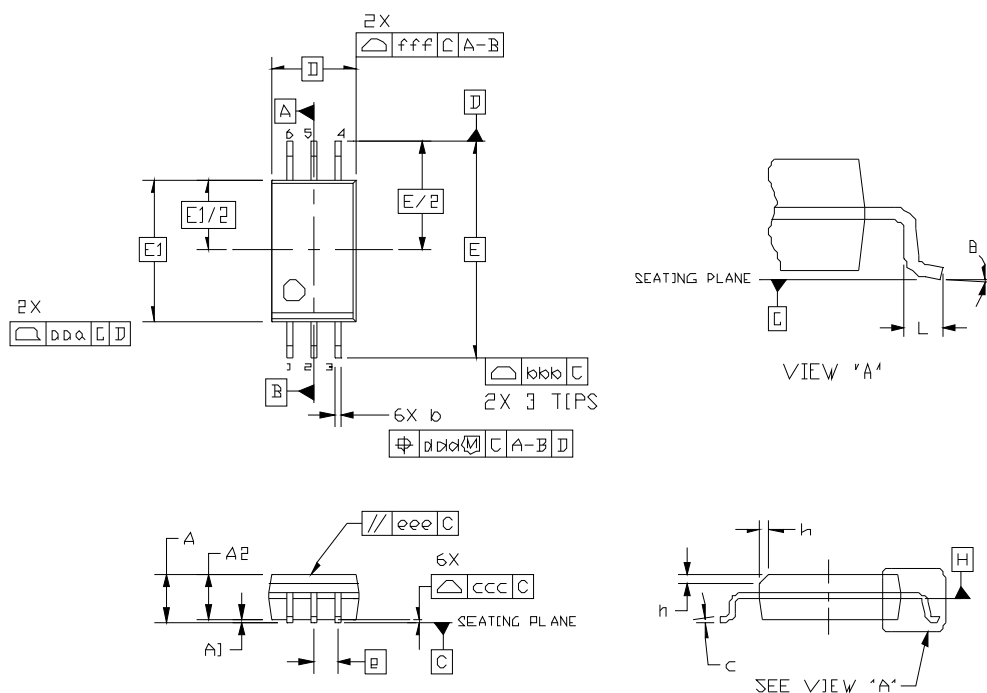


Figure 21. SDIP6 Package

Table 20. SDIP6 Package Diagram Dimensions

| Dimension | Min | Max |
|-----------|-----------|------|
| A | — | 2.65 |
| A1 | 0.10 | 0.30 |
| A2 | 2.05 | — |
| b | 0.31 | 0.51 |
| c | 0.20 | 0.33 |
| D | 4.58 BSC | |
| E | 11.50 BSC | |
| E1 | 7.50 BSC | |
| e | 1.27 BSC | |
| L | 0.40 | 1.27 |
| h | 0.25 | 0.75 |

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

Table 20. SDIP6 Package Diagram Dimensions (Continued)

| Dimension | Min | Max |
|------------------|------------|------------|
| θ | 0° | 8° |
| aaa | — | 0.10 |
| bbb | — | 0.33 |
| ccc | — | 0.10 |
| ddd | — | 0.25 |
| eee | — | 0.10 |
| fff | — | 0.20 |

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

15. Land Pattern: SDIP6

Figure 22 illustrates the recommended land pattern details for the Si87xx in an SDIP6 package. Table 21 lists the values for the dimensions shown in the illustration.

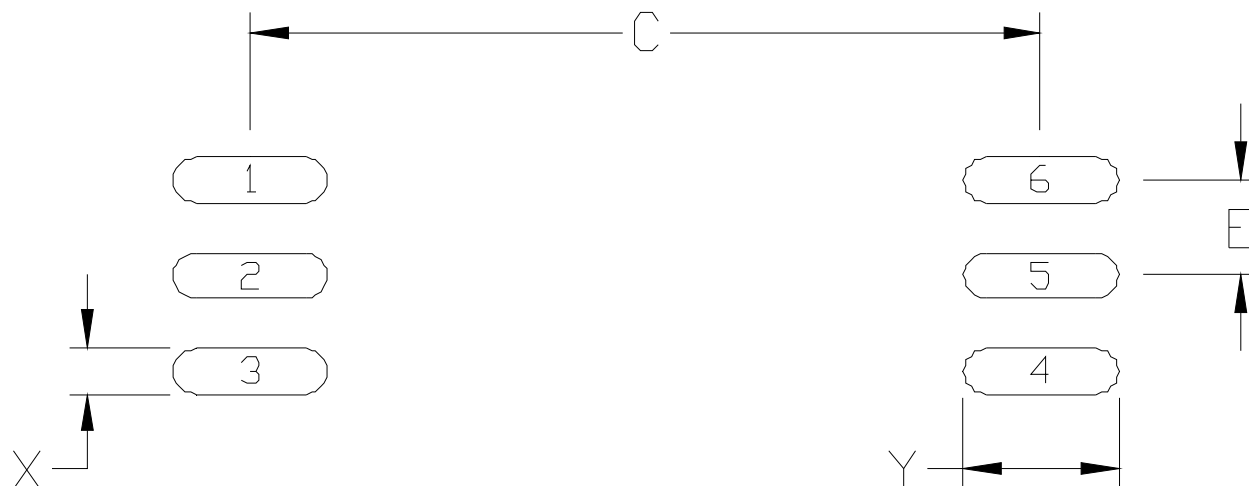


Figure 22. SDIP6 Land Pattern

Table 21. SDIP6 Land Pattern Dimensions*

| Dimension | Min | Max |
|--|----------|-------|
| C | 10.45 | 10.50 |
| E | 1.27 BSC | |
| X | 0.55 | 0.60 |
| Y | 2.00 | 2.05 |
| *Note: This Land Pattern Design is based on the IPC-7351 specification. | | |

16. Package Outline: LGA8

Figure 23 illustrates the package details for the Si87xx in an LGA8 package. Table 22 lists the values for the dimensions shown in the illustration.

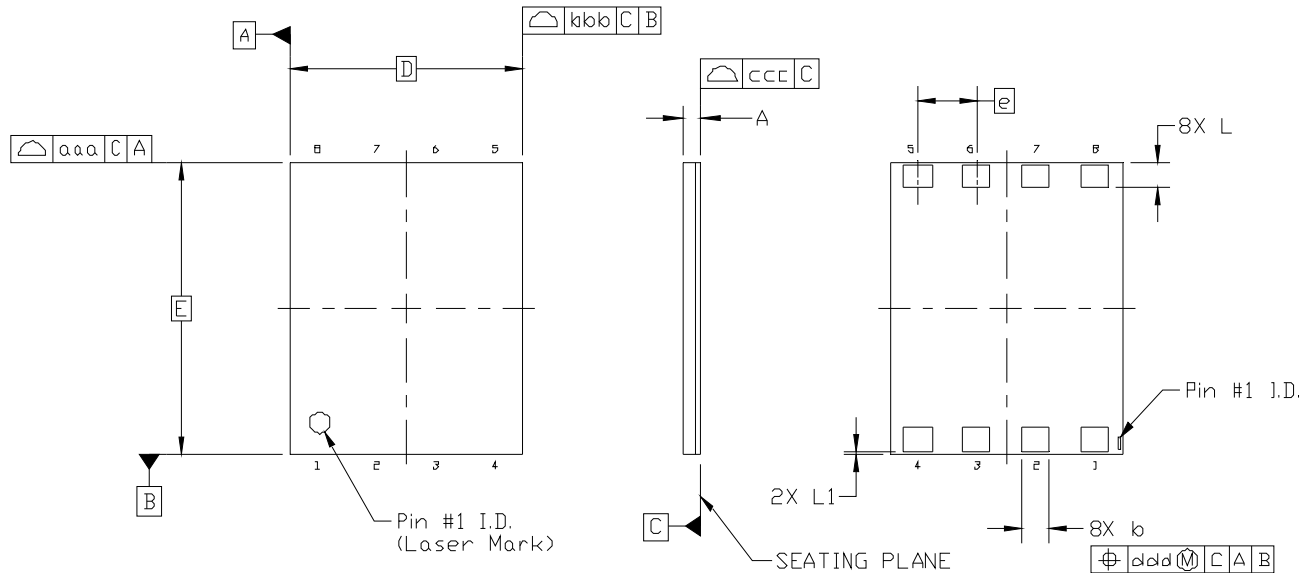


Figure 23. LGA8 Package

Table 22. Package Diagram Dimensions

| Dimension | Min | Nom | Max |
|--|------------|------|------|
| A | 0.74 | 0.84 | 0.94 |
| b | 1.15 | 1.20 | 1.25 |
| D | 10.00 BSC. | | |
| e | 2.54 BSC. | | |
| E | 12.50 BSC. | | |
| L | 1.05 | 1.10 | 1.15 |
| L1 | 0.05 | 0.10 | 0.15 |
| aaa | — | — | 0.10 |
| bbb | — | — | 0.10 |
| ccc | — | — | 0.10 |
| ddd | — | — | 0.10 |
| Notes: | | | |
| 1. All dimensions shown are in millimeters (mm) unless otherwise noted. | | | |
| 2. Dimensioning and Tolerancing per ANSI Y14.5M-1994. | | | |
| 3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components. | | | |

17. Land Pattern: LGA8

Figure 24 illustrates the recommended land pattern details for the Si87xx in an LGA8 package. Table 23 lists the values for the dimensions shown in the illustration.

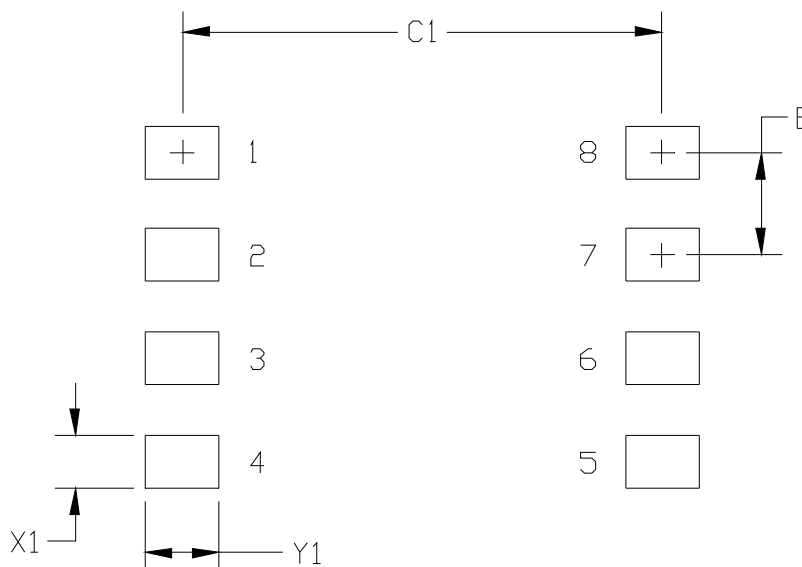


Figure 24. LGA8 Land Pattern

Table 23. LGA8 Land Pattern Dimensions

| Dimension | Feature | (mm) |
|-----------|--------------------|-------|
| C1 | Pad Column Spacing | 11.80 |
| E | Pad Row Pitch | 2.54 |
| X1 | Pad Width | 1.30 |
| Y1 | Pad Length | 1.80 |

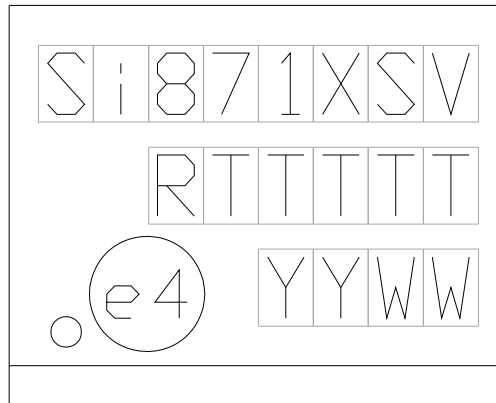
Notes:

1. This Land Pattern Design is based on IPC-7351 specifications.
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

Si87xx

18. Top Markings

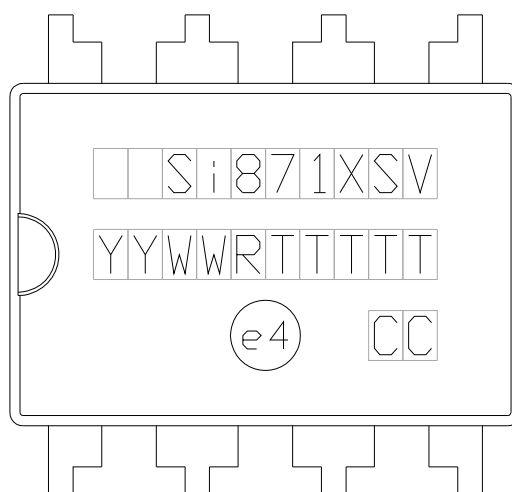
18.1. Top Marking (8-Pin Narrow Body SOIC)



18.2. Top Marking Explanation (8-Pin Narrow Body SOIC)

| | | |
|------------------------|---|---|
| Line 1 Marking: | Customer Part Number | Si871 = Isolator product series X = Output configuration 0 = open collector output only 1 = open collector output w/ internal pull-up 2 = open collector output w/ output enable S = Performance Grade: A = 15 Mbps, 20 kV/μs minimum CMTI B = 15 Mbps, 35 kV/μs minimum CMTI C = 1 Mbps, 20 kV/μs minimum CMTI V = Insulation rating C = 3.75 kV |
| Line 2 Marking: | RTTTTT = Mfg Code | Manufacturing Code from the Assembly Purchase Order form. “R” indicates revision. |
| Line 3 Marking: | Circle = 43 mils Diameter Left-Justified | “e4” Pb-Free Symbol |
| | YY = Year WW = Work Week | Assigned by the Assembly House. Corresponds to the year and work week of the mold date. |

18.3. Top Marking (DIP8)

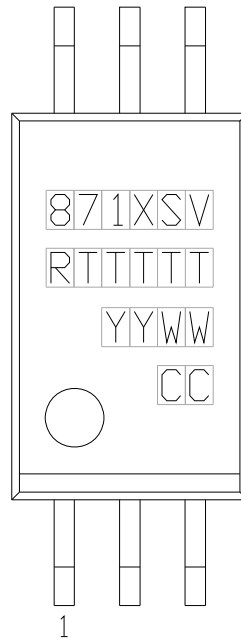


18.4. Top Marking Explanation (DIP8)

| | | |
|------------------------|---|---|
| Line 1 Marking: | Customer Part Number | Si871 = Isolator product series X = Output configuration 0 = open collector output only 1 = open collector output w/ internal pull-up 2 = open collector output w/ output enable S = Performance Grade: A = 15 Mbps, 20 kV/ μ s minimum CMTI B = 15 Mbps, 35 kV/ μ s minimum CMTI C = 1 Mbps, 20 kV/ μ s minimum CMTI V = Insulation rating C = 3.75 kV |
| Line 2 Marking: | YY = Year WW = Work Week | Assigned by the Assembly House. Corresponds to the year and work week of the mold date. |
| | RTTTTT = Mfg Code | Manufacturing Code from the Assembly Purchase Order form. "R" indicates revision. |
| Line 3 Marking: | Circle = 51 mils Diameter Center-Justified | "e4" Pb-Free Symbol |
| | Country of Origin (Iso-Code Abbreviation) | CC |

Si87xx

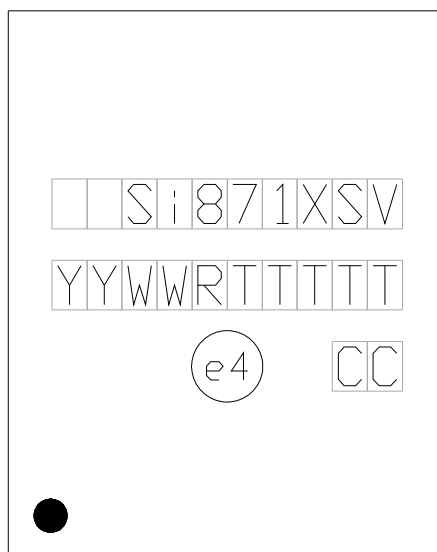
18.5. Top Marking (SDIP6)



18.6. Top Marking Explanation (SDIP6)

| | | |
|------------------------|--|---|
| Line 1 Marking: | Device | <p>871 = Isolator product series</p> <p>X = Output configuration</p> <ul style="list-style-type: none"> 0 = open collector output only 1 = open collector output w/ internal pull-up 2 = open collector output w/ output enable <p>S = Performance Grade:</p> <ul style="list-style-type: none"> A = 15 Mbps, 20 kV/μs minimum CMTI B = 15 Mbps, 35 kV/μs minimum CMTI C = 1 Mbps, 20 kV/μs minimum CMTI <p>V = Insulation rating</p> <ul style="list-style-type: none"> C = 3.75 kV; D = 5.0 kV |
| Line 2 Marking: | RTTTTT = Mfg Code | <p>Manufacturing Code from the Assembly Purchase Order form.</p> <p>“R” indicates revision.</p> |
| Line 3 Marking: | YY = Year WW = Work Week | Assigned by the Assembly House. Corresponds to the year and work week of the mold date. |
| Line 4 Marking: | Country of Origin (Iso-Code Abbreviation) | CC |

18.7. Top Marking (LGA8)



18.8. Top Marking Explanation (LGA8)

| | | |
|------------------------|---|---|
| Line 1 Marking: | Device Part Number | Si871 = Isolator product series X = Output configuration 0 = open collector output only 1 = open collector output w/ internal pull-up 2 = open collector output w/ output enable S = Performance Grade: A = 15 Mbps, 20 kV/ μ s minimum CMTI B = 15 Mbps, 35 kV/ μ s minimum CMTI C = 1 Mbps, 20 kV/ μ s minimum CMTI V = Insulation rating C = 3.75 kV; D = 5.0 kV |
| Line 2 Marking: | YY = Year WW = Work Week | Assigned by the Assembly House. Corresponds to the year and work week of the assembly release. |
| | RTTTTT = Mfg Code | Manufacturing Code from the Assembly Purchase Order form. "R" indicates revision. |
| Line 3 Marking: | Circle = 1.6 mm Diameter Center-Justified | "e4" Pb-Free Symbol |
| | Country of Origin ISO Code Abbreviation | CC |
| Line 4 Marking: | Circle = 0.75 mm Diameter Lower Left-Justified | Pin 1 Identifier |

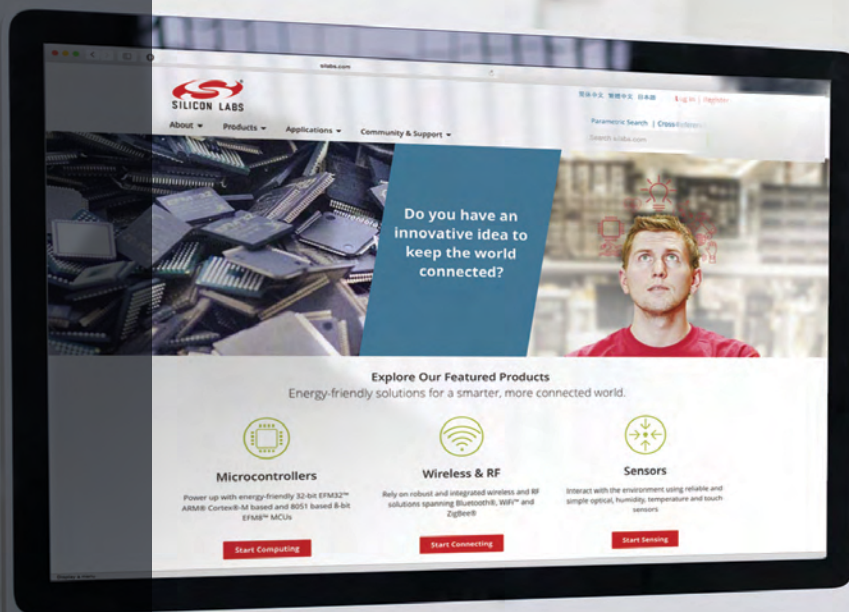
DOCUMENT CHANGE LIST

Revision 0.5 to Revision 1.0

- Updated various specs in Table 2 on page 4.
- Added Figure 1 on page 6.
- Added Figure 2 on page 7.
- Added Figure 8 on page 15.
- Updated various specs in Table 10 on page 16.
- Removed “pending” throughout.
- Added references to “CQC” throughout.
- Added references to “AEC-Q100 qualified” throughout.
- Updated all Top Marking figures and descriptions.

Revision 1.0 to Revision 1.1

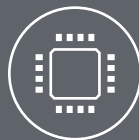
- Updated Figure 1 on page 6.
- Updated Ordering Guide Table 15 on page 22.
 - Removed references to moisture sensitivity levels from table note.



Smart.
Connected.
Energy-Friendly



Products
www.silabs.com/products



Quality
www.silabs.com/quality



Support and Community
community.silabs.com

Disclaimer

Silicon Laboratories intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Laboratories products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Laboratories reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Laboratories shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products must not be used within any Life Support System without the specific written consent of Silicon Laboratories. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Laboratories products are generally not intended for military applications. Silicon Laboratories products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.

Trademark Information

Silicon Laboratories Inc., Silicon Laboratories, Silicon Labs, SiLabs and the Silicon Labs logo, CMEMS®, EFM, EFM32, EFR, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZMac®, EZRadio®, EZRadioPRO®, DSPLL®, ISOmodem®, Precision32®, ProSLIC®, SiPHY®, USBXpress® and others are trademarks or registered trademarks of Silicon Laboratories Inc. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.



Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

<http://www.silabs.com>